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10/595,158	03/09/2006	Hajime Kimura	12732-0325US1	3518

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FISH & RICHARDSON P.C. (DC)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
ZUBAJLO, JENNIFER L	
ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
12/09/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/595,158	KIMURA, HAJIME	
	Examiner	Art Unit	
	JENNIFER ZUBAJLO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/20/11*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-18,20-24 and 26-36* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-18,20-24 and 26-36* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-18, 20-24, and 26-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Masanobu Oomura (Patent No.: US 6,693,388 B2).

As to claim 1, Oomura teaches a semiconductor device comprising: a transistor comprising a source, a drain and a gate (see fig. 1 – transistor T3); a current source electrically connected to the gate and one of the source and the drain (see fig. 1 – current source Id – note that it is obvious that current source Id is electrically connected to T3 throughT5 and T4); and a precharge circuit comprising a first terminal and a second terminal, wherein both the first terminal and the second terminal are electrically connected to the gate and the one of the source and the drain (see fig. 1- note that it is obvious that both terminals are electrically connected to the gate of T3 through transistors T5 and T4 and through T2 and T1).

As to claim 6, Oomura teaches a semiconductor device comprising: a transistor comprising a source, a drain, and a gate (see fig. 1 – transistor T3); a current source

electrically connected to the gate and one of the source and the drain (see fig. 1 – current source Id – note that it is obvious that current source Id is electrically connected to T3 through T5 and T4); a charge supply means (see fig. 1 – Vdd); and a precharge circuit configured to supply a charge to the transistor, the precharge circuit comprising: a comparison control circuit having an output terminal, a first input terminal, and a second input terminal electrically connected to the gate and the one of the source and the drain (see fig. 1 – comparison control circuit AMP1, where terminal 2 is obviously electrically connected to current source Id line to T3 through T5 and T4); and a switch electrically connected to the output terminal, wherein the charge supply means is electrically connected to the gate and the source and the drain through the switch (see fig. 1 – charge supply Vdd is obviously electrically connected to gate of T3 through switch T1).

As to claim 12, Oomura teaches a semiconductor device comprising: a transistor comprising a source, a drain and a gate (see fig. 1 – transistor T3); a capacitor electrically connected to the gate and one of the source and the drain (see fig.1 - capacitor C connected to T3 through T1); a current source electrically connected to the gate and the one of the source and the drain (see fig. 1 – current source Id – note that it is obvious that current source Id is electrically connected to T3 through T5 and T4); a charge supply means (see fig. 1 – Vdd); and a precharge circuit configured to supply a charge to the transistor, the precharge circuit comprising: a comparison control circuit having an output terminal, a first input terminal, and a second input terminal electrically

connected to the gate and the one of the source and the drain (see fig. 1 – comparison control circuit AMP1, where terminal 2 is obviously electrically connected to current source Id line to T3 through T5 and T4); and a switch electrically connected to the output terminal, wherein the charge supply means is electrically connected to the gate and the one of the source and the drain through the switch (see fig. 1 – charge supply Vdd is obviously electrically connected to gate of T3 through switch T1).

As to claim 18, Oomura teaches a display device comprising: a light emitting element (see fig. 1 – OLED); a transistor comprising a source, a drain and a gate, and electrically connected to the light emitting element (see fig. 1 – T3); a current source electrically connected to the gate and one of the source and the drain (see fig. 1 – current source Id – note that it is obvious that current source Id is electrically connected to T3 through T5 and T4); and a precharge circuit comprising a first terminal and a second terminal, wherein both the first terminal and the second terminal are electrically connected to the gate and the one of the source and the drain (see fig. 1- note that it is obvious that both terminals are electrically connected to the gate of T3 through transistors T5 and T4 and through T2 and T1).

As to claim 24, Oomura teaches a display device comprising: a light emitting element (see fig. 1 – OLED); a transistor comprising a source, a drain and a gate, and electrically connected to the light emitting element (see fig. 1 – T3); a current source electrically connected to the gate and one of the source and the drain (see fig. 1 –

current source Id – note that it is obvious that current source Id is electrically connected to T3 through T5 and T4); a charge supply means (see fig. 1 – Vdd); and a precharge circuit configured to supply a charge to the transistor, the precharge circuit comprising: a comparison control circuit having an output terminal, a first input terminal, and a second input terminal electrically connected to the gate and the one of the source and the drain (see fig. 1 – comparison control circuit AMP1, where terminal 2 is obviously electrically connected to current source Id line to T3 through T5 and T4); and a switch electrically connected to the output terminal, wherein the charge supply means is electrically connected to the gate and the source and the drain through the switch (see fig. 1 – charge supply Vdd is obviously electrically connected to gate of T3 through switch T1).

As to claim 31, Oomura teaches a display device comprising: a light emitting element (see fig. 1 – OLED); a transistor comprising a source, a drain and a gate (see fig. 1 – T3); a capacitor electrically connected to the gate and one of the source and the drain (see fig.1 - capacitor C connected to T3 through T1); a current source electrically connected to the gate and the one of the source and the drain (see fig. 1 – current source Id – note that it is obvious that current source Id is electrically connected to T3 through T5 and T4); a charge supply means (see fig. 1 – Vdd); and a precharge circuit configured to supply a charge to the transistor, the precharge circuit comprising: a comparison control circuit having an output terminal, a first input terminal, and a second input terminal electrically connected to the gate and the one of the source and

the drain (see fig. 1 – comparison control circuit AMP1, where terminal 2 is obviously electrically connected to current source Id line to T3 through T5 and T4); and

a switch electrically connected to the output terminal, wherein the charge supply means is electrically connected to the gate and the one of the source and the drain through the switch, wherein the light emitting element is electrically connected to any one of the source and the drain (see fig. 1 – OLED connected to T3, charge supply Vdd is obviously electrically connected to gate of T3 through switch T1).

As to claim 2, Oomura teaches semiconductor device according to Claim 1 (see above rejection), wherein the precharge circuit comprises: a comparison control circuit for the comparison between the potential of a first input terminal and the potential of a second input terminal (see fig. 1 – AMP1); and a switch controlled by the comparison control circuit (see either T2 or T1 which are both switches controlled by the comparison control circuit).

As to claim 3, Oomura teaches a semiconductor device according to Claim 2 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 4, Oomura teaches a semiconductor device according to Claim 2 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and

well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 5, Oomura teaches an electronic apparatus having the semiconductor device according to Claim 1 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

As to claim 7, Oomura teaches a semiconductor device according to Claim 6 (see above rejection), wherein the charge supply means is a second current source (see fig. 1 – Vdd and note that it is well known in the art to use either current or voltage sources as charge supply would be obvious to substitute a current source in place of a voltage source).

As to claim 8, Oomura teaches a semiconductor device according to Claim 6 (see above rejection), wherein the charge supply means is a power source (see fig. 1 - Vdd).

As to claim 9, Oomura teaches a semiconductor device according to Claim 6 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 10, Oomura teaches a semiconductor device according to Claim 6 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 11, Oomura teaches an electronic apparatus having the semiconductor device according to Claim 6 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

As to claim 13, Oomura teaches a semiconductor device according to Claim 12 (see above rejection), wherein the charge supply means is a second current source (see fig. 1 – Vdd and note that it is well known in the art to use either current or voltage sources as charge supply would be obvious to substitute a current source in place of a voltage source).

As to claim 14, Oomura teaches a semiconductor device according to Claim 12 (see above rejection), wherein the charge supply means is a power source (see fig. 1 – Vdd).

As to claim 15, Oomura teaches a semiconductor device according to Claim 12 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 16, Oomura teaches the semiconductor device according to Claim 12 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 17, Oomura teaches an electronic apparatus having the semiconductor device according to Claim 12 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

As to claim 20, Oomura teaches a display device according to Claim 18 (see above rejection), wherein the precharge circuit comprises: a comparison control circuit for the comparison between the potential of the first terminal and the potential of the second terminal (see fig. 1 – AMP1); and a switch controlled by the comparison control circuit (see fig. 1 – switch T2 or T1).

As to claim 21, Oomura teaches a display device according to Claim 20 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 22, Oomura teaches a display device according to Claim 20 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 23, Oomura teaches an electronic apparatus having the display device according to Claim 18 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

As to claim 26, Oomura teaches a display device according to Claim 24 (see above rejection), wherein the charge supply means is a second current source (see fig. 1 – Vdd and note that it is well known in the art to use either current or voltage sources as charge supply would be obvious to substitute a current source in place of a voltage source).

As to claim 27, Oomura teaches a display device according to Claim 24 (see above rejection), wherein the charge supply means is a power source (see fig. 1 – Vdd).

As to claim 28, Oomura teaches a display device according to Claim 24 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 29, Oomura teaches a display device according to Claim 24 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 30, Oomura teaches an electronic apparatus having the display device according to Claim 24 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop

personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

As to claim 32, Oomura teaches a display device according to Claim 31 (see above rejection), wherein the charge supply means is a second current source (see fig. 1 – Vdd and note that it is well known in the art to use either current or voltage sources as charge supply would be obvious to substitute a current source in place of a voltage source).

As to claim 33, Oomura teaches a display device according to Claim 31 (see above rejection), wherein the charge supply means is a power source (see fig. 1 – Vdd).

As to claim 34, Oomura teaches a display device according to Claim 31 (see above rejection), wherein the comparison control circuit comprises an operational amplifier (see fig. 1 – AMP1).

As to claim 35, Oomura teaches a display device according to Claim 31 (see above rejection), wherein the comparison control circuit comprises a chopper inverter comparator (see fig 1 and note chopper inverter comparators are obvious and well known substitutions for operational amplifiers in the art because they perform the same function).

As to claim 36, Oomura teaches an electronic apparatus having the display device according to Claim 31 (see above rejection), wherein the electronic apparatus is selected from the group consisting of a light emitting device, a digital still camera, laptop personal computer, a mobile computer, a portable image reproducing device, a goggle type display, a video camera and a portable phone (see fig. 1 – OLED).

Response to Arguments

3. Applicant's arguments filed 9/20/11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER ZUBAJLO whose telephone number is (571)270-1551. The examiner can normally be reached on Monday-Friday, 10 am - 7 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jennifer Zubajlo/
Examiner, Art Unit 2629
11/22/11

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629